

REV: 1.0 1

SHEET

TITLE

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02	BOM & PCB MODIFY HISTORY
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05	CPU LGA1156-B
06	CPU LGA1156-C
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12	PCH HOST ,SATA ,PCI
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24	DDR 15V ,PWR SEQ
25	CPU VAXG PWM ISL6314CRZ
26	CPU VTT PWM ISL6322G
27	VCORE PWM ISL6334CR

SHEET

TITLE

[illegible]

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GA-H55-UD3H

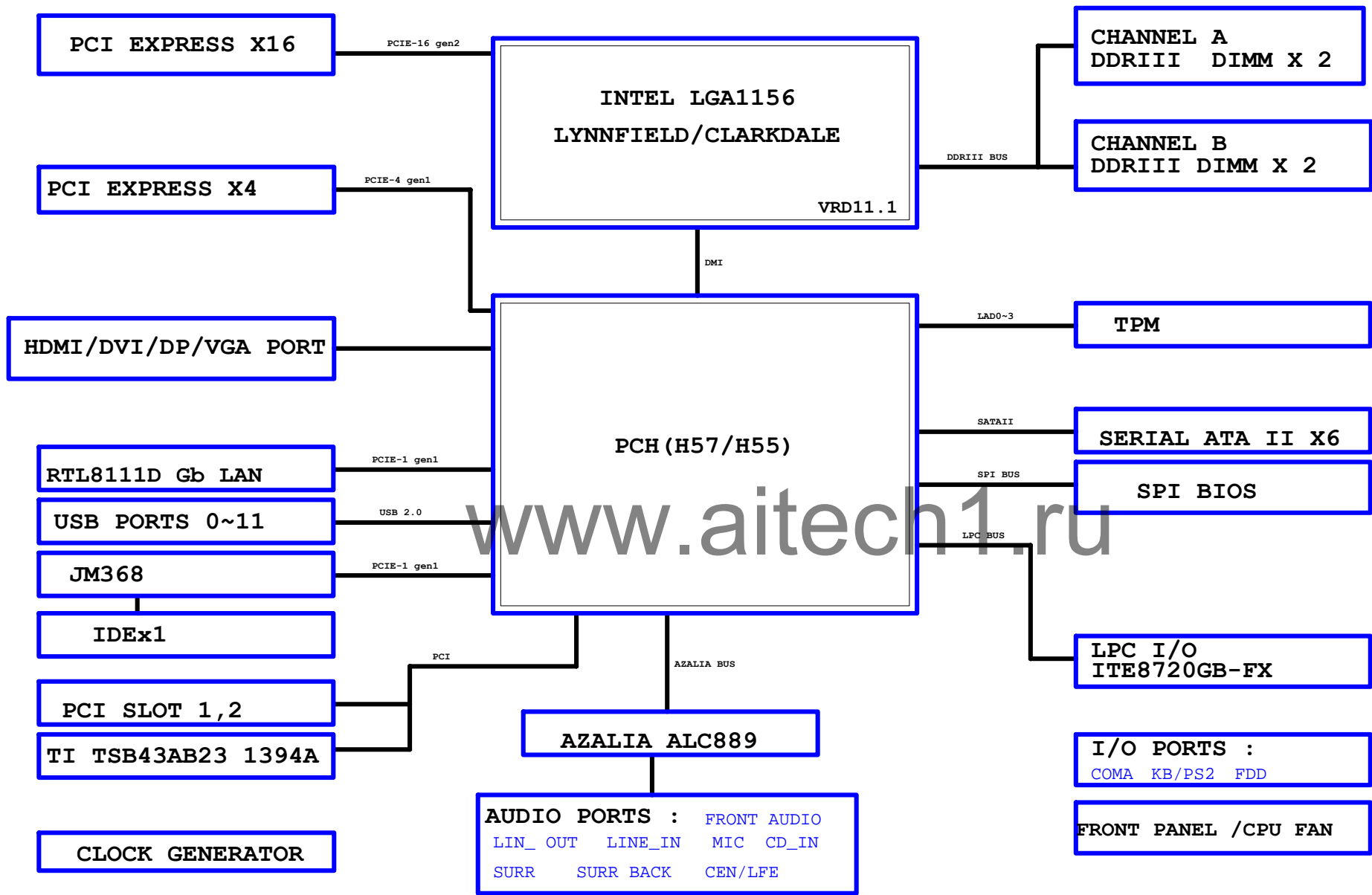
Circuit or PCB layout change
for next version

Component value change history

2009/08/27

[illegible][illegible]

BLOCK DIAGRAM



LGA1156A			
MAAA0	AW18	SA_MA[0]	SA_DQS[0]
MAAA1	AY15	SA_MA[1]	SA_DQS[1]
MAAA2	AW15	SA_MA[2]	SA_DM[0]
MAAA3	AU15	SA_MA[3]	SA_DQ[0]
MAAA4	AW14	SA_MA[4]	SA_DQ[1]
MAAA5	AY13	SA_MA[5]	SA_DQ[2]
MAAA6	AV14	SA_MA[6]	SA_DQ[3]
MAAA7	AW13	SA_MA[7]	SA_DQ[4]
MAAA8	AU14	SA_MA[8]	SA_DQ[5]
MAAA9	AW12	SA_MA[9]	SA_DQ[6]
MAAA10	AT19	SA_MA[10]	SA_DQ[7]
MAAA11	AU13	SA_MA[11]	SA_DQS[11]
MAAA12	AW11	SA_MA[12]	SA_DQS[11]
MAAA13	AU24	SA_MA[13]	SA_DM[1]
MAAA14	AT11	SA_MA[14]	SA_DQ[8]
MAAA15	AR10	SA_MA[15]	SA_DQ[9]
[7] -SWEA	-SWEA	AT22	SA_WE#
[7] -SCASA	-SCASA	AU22	SA_CAS#
[7] -SRASA	-SRASA	AT20	SA_RAS#
[7] SBAA0	SBAA0	AV20	SA_BS[0]
[7] SBAA1	SBAA1	AU19	SA_BS[1]
[7] SBAA2	SBAA2	AU12	SA_BS[2]
[7] -CSA0	-CSA0	AV21	SA_CS#0
[7] -CSA1	-CSA1	AW24	SA_CS#1
[7] -CSA2	-CSA2	AU21	SA_CS#2
[7] -CSA3	-CSA3	AU23	SA_CS#3
[7] CKEA0	CKEA0	AU10	SA_CKE[0]
[7] CKEA1	CKEA1	AW10	SA_CKE[1]
[7] CKEA2	CKEA2	AV10	SA_CKE[2]
[7] CKEA3	CKEA3	AY10	SA_CKE[3]
MODT_A0	AV23	SA_ODT[0]	
MODT_A1	AV24	SA_ODT[1]	
MODT_A2	AW23	SA_ODT[2]	
MODT_A3	AY24	SA_ODT[3]	
[7] DCLKA0	DCLKA0	AR22	SA_CK[0]
[7] -DCLKA0	-DCLKA0	AR21	SA_CK#0
[7] DCLKA1	DCLKA1	AP18	SA_CK[1]
[7] -DCLKA1	-DCLKA1	AN18	SA_CK#1
[7] DCLKA2	DCLKA2	AN21	SA_CK[2]
[7] -DCLKA2	-DCLKA2	AP21	SA_CK#2
[7] DCLKA3	DCLKA3	AP19	SA_CK[3]
[7] -DCLKA3	-DCLKA3	AN19	SA_CK#3
[7,8] -DDR3_RST	-DDR3_RST	AV8	SM_DRAMRST#
TP1	AK22	SA_CS#4	
TP1	AM22	SA_CS#5	
TP1	AL23	SA_CS#6	
TP1	AK23	SA_CS#7	
AL10	SA_DQS[8]		
AM10	SA_DQS#8		
AP10	SA_ECC_CB[0]		
AR11	SA_ECC_CB[1]		
AP11	SA_ECC_CB[2]		
AK9	SA_ECC_CB[3]		
AL9	SA_ECC_CB[4]		
AK11	SA_ECC_CB[5]		
AM11	SA_ECC_CB[6]		
AM11	SA_ECC_CB[7]		
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SA_DQS[6]	SA_DQS[6]	SA_DQS[6]	SA_DQS[6]
SA_DQS#6	SA_DQS#6	SA_DQS#6	SA_DQS#6
SA_DM[6]	SA_DM[6]	SA_DM[6]	SA_DM[6]
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SA_DQS#7	SA_DQS#7	SA_DQS#7	SA_DQS#7
SA_DM[7]	SA_DM[7]	SA_DM[7]	SA_DM[7]
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SA_DQ[62]	SA_DQ[62]	SA_DQ[62]	SA_DQ[62]
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DDR_A

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LGA1156[10SC1-F01156-01R]

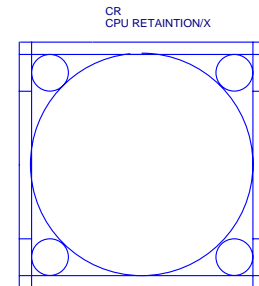
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[7] -DQSA[0..7]	-DQSA[0..7]
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[8] -DQSB[0..7]	-DQSB[0..7]
[7] MODT_A[0..3]	MODT_A[0..3]
[8] MODT_B[0..3]	MODT_B[0..3]
[7] MAAA[0..15]	MAAA[0..15]
[8] MAAB[0..15]	MAAB[0..15]
[7] DMA[0..7]	DMA[0..7]
[8] DMB[0..7]	DMB[0..7]
[7] MDA[0..63]	MDA[0..63]
[8] MDB[0..63]	MDB[0..63]

LGA1156B			
MAAB0	AU20	SB_MA[0]	SB_DQS[0]
MAAB1	AU18	SB_MA[1]	SB_DQS[1]
MAAB2	AV18	SB_MA[2]	SB_DM[0]
MAAB3	AU17	SB_MA[3]	SB_DQ[0]
MAAB4	AY18	SB_MA[4]	SB_DQ[1]
MAAB5	AV17	SB_MA[5]	SB_DQ[2]
MAAB6	AW17	SB_MA[6]	SB_DQ[3]
MAAB7	AU16	SB_MA[7]	SB_DQ[4]
MAAB8	AT17	SB_MA[8]	SB_DQ[5]
MAAB9	AY25	SB_MA[9]	SB_DQ[6]
MAAB10	AV25	SB_MA[10]	SB_DQ[7]
MAAB11	AW16	SB_MA[11]	SB_DQS[11]
MAAB12	AW15	SB_MA[12]	SB_DQS[11]
MAAB13	AW28	SB_MA[13]	SB_DM[1]
MAAB14	AY12	SB_MA[14]	SB_DQ[8]
MAAB15	AV11	SB_MA[15]	SB_DQ[9]
[8] -SWEB	-SWEB	AW26	SB_WE#
[8] -SCASB	-SCASB	AW26	SB_CAS#
[8] -SRASB	-SRASB	AW26	SB_RAS#
[8] SBAB0	SBAB0	AU25	SB_BS[0]
[8] SBAB1	SBAB1	AW25	SB_BS[1]
[8] SBAB2	SBAB2	AV12	SB_BS[2]
[8] -CSB0	-CSB0	AY27	SB_CS#0
[8] -CSB1	-CSB1	AW26	SB_CS#1
[8] -CSB2	-CSB2	AV29	SB_CS#2
[8] -CSB3	-CSB3	AV29	SB_CS#3
[8] CKEB0	CKEB0	AW8	SB_CKE[0]
[8] CKEB1	CKEB1	AV9	SB_CKE[1]
[8] CKEB2	CKEB2	AU9	SB_CKE[2]
[8] CKEB3	CKEB3	AV9	SB_CKE[3]
MODT_B0	AU27	SB_ODT[0]	
MODT_B1	AU29	SB_ODT[1]	
MODT_B2	AV27	SB_ODT[2]	
MODT_B3	AU27	SB_ODT[3]	
TP12	AM23	SB_CS#4	
TP13	AM24	SB_CS#5	
TP15	AK24	SB_CS#6	
TP17	AK24	SB_CS#7	
AR14	SA_DQS[8]		
AR13	SA_DQS#8		
AR12	SA_ECC_CB[0]		
AT13	SA_ECC_CB[1]		
AN15	SA_ECC_CB[2]		
AP14	SA_ECC_CB[3]		
AM12	SA_ECC_CB[4]		
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DDR_B

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LGA1156[10SC1-F01156-01R]



Need check the new CPU ME

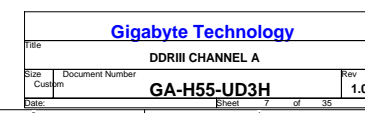
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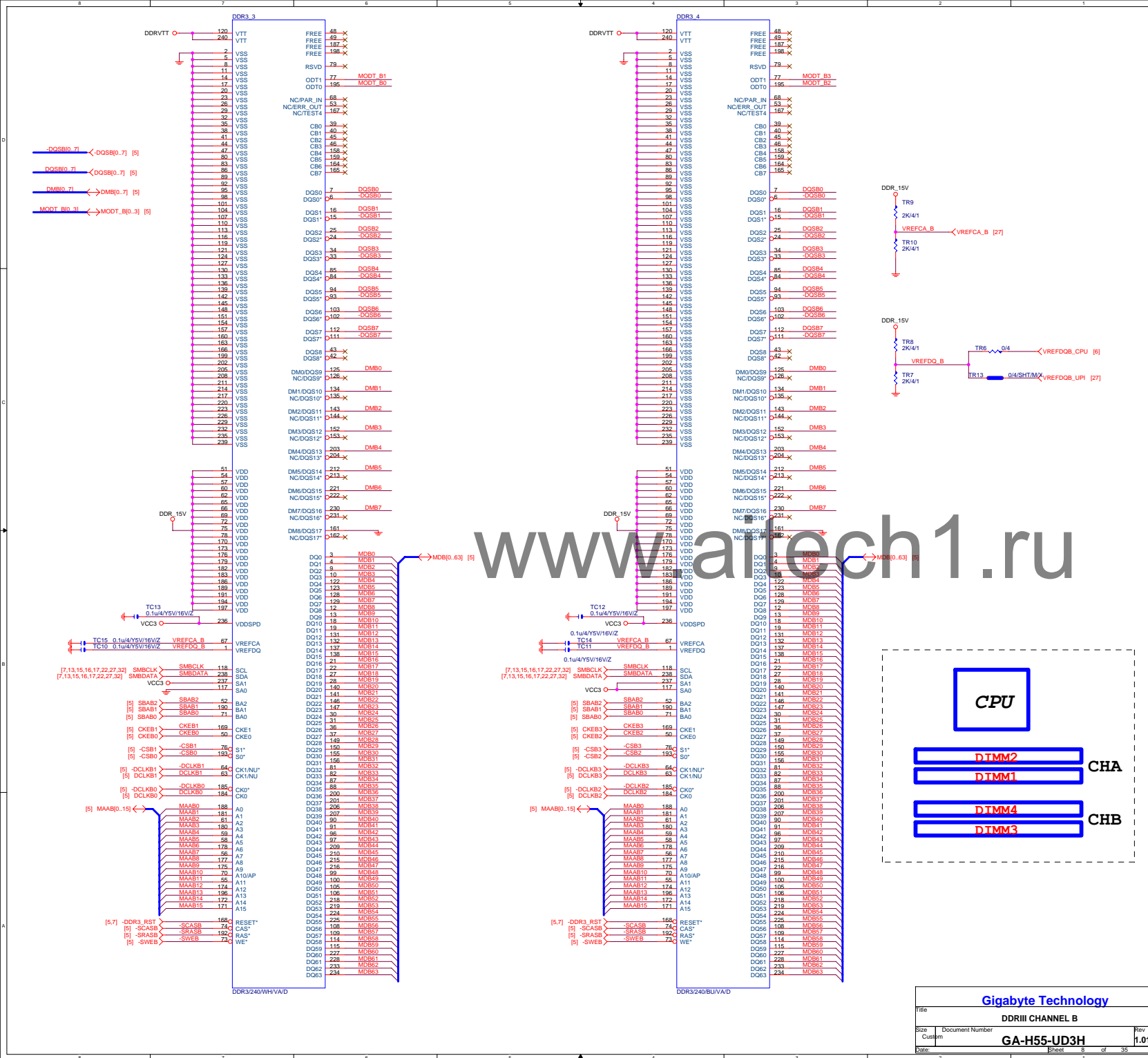


PLATE+LHM[12KRC-0F0001-01R]

Gigabyte Technology

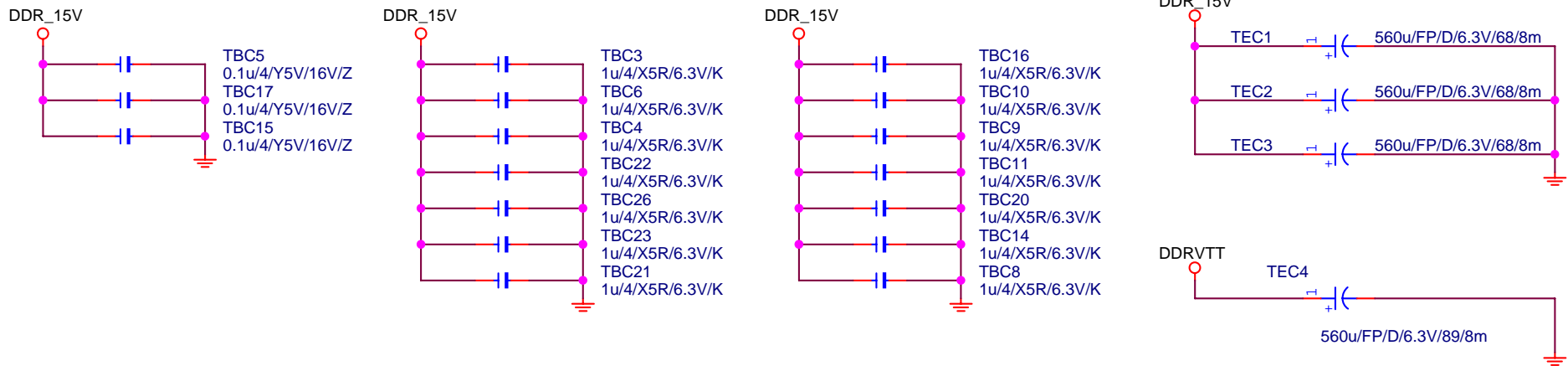
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CPU LGA1156-B		
Size	Document Number	Rev
Custom	GA-H55-UD3H	1.01
Date:	Monday, December 21, 2009	Sheet 5 of 35



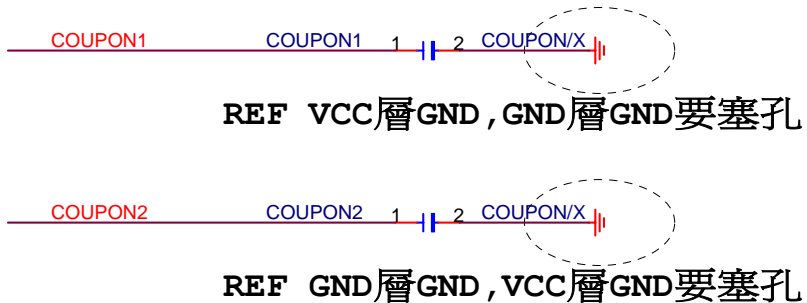
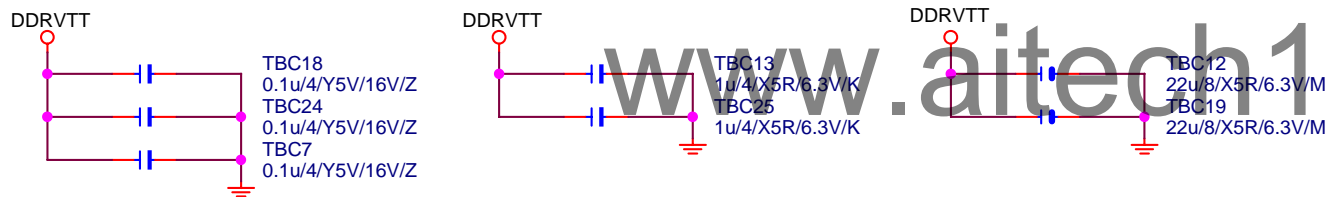


DDR TERMINATION CHANNEL A/B

DDR15V Decouple



DDRVTT Decouple



Gigabyte Technology			
Title			
DDRIII POWER CAP			
Size A	Document Number	GA-H55-UD3H	Rev 1.01
Date:	Monday, December 21, 2009	Sheet 9 of 35	

DMI:12/5/5/5/12
Impedance=80 +- 17.5%

USB:15/4.5/7.5/4.5/15
Impedance=90+- 15%

PCHE

Impedance=80 +- 17.5%

PCIE X1 :15/5/5/5/15

PCIE X4

PCIE X1

LAN

电容要靠近 slot 端
H55 PCIE (7,8) -->N/A

PCH_HS

PCH_HS[12SP2-030030-C1R]

PCHB

DMI

USB

PCI-E

H55/B3

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H55-->PORT6,7:N/A

OC[3:0]# for
Device 29
(ports 0-7)
OC[7:4]# for
Device 26
(ports 8-13)

USB OC# Configure	
OC0#	USB0,1(F_USB1)
OC1#	USB2,3(F_USB2)
OC2#	USB4,5(F_USB3)
OC3#	USB6,7(F_USB4) H55-->N/A
OC4#	USB8,9(USB_LAN)
OC5#	USB10~11(USB_1394_ESATA)
OC6#	USB12~13(KB_USB)
OC7#	GPIO14

NV_ALE	
Hi	Enable Danbury
Lo	Disable Danbury

Intel anti theft technolgy

NV_ALE

NV_CLE

NVRAM

H55/B3

Impedance=50+- 15%

ONFI: NV_DQ 4/5

NV_DQS 4/10

NV_CTRL 4/10

NV_CK 4/15

NV_PCH

NV_PCH

NV_PCH

NV_PCH

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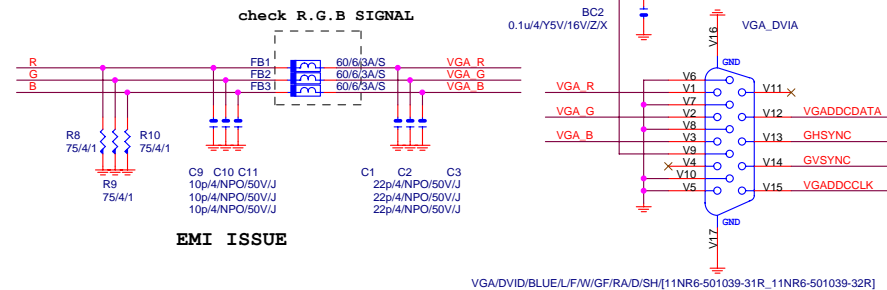
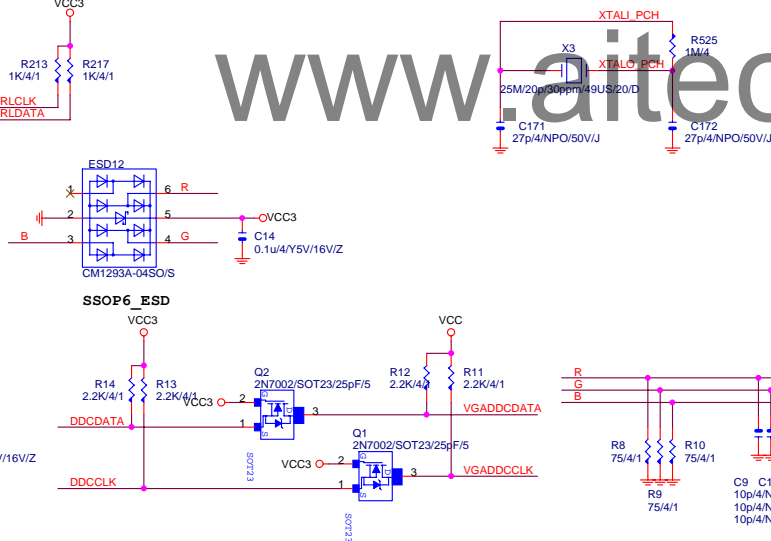
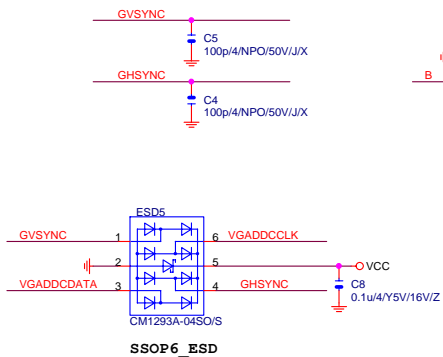
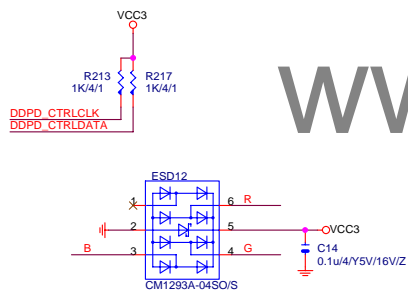
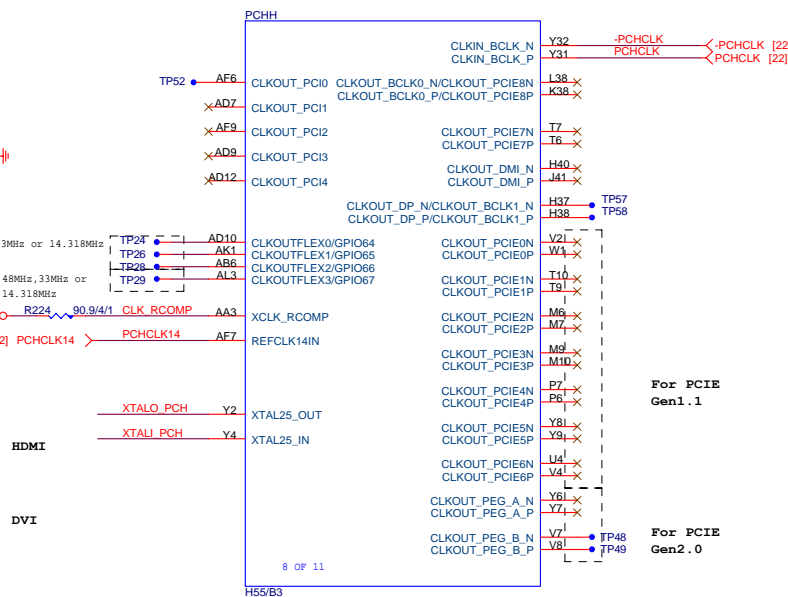
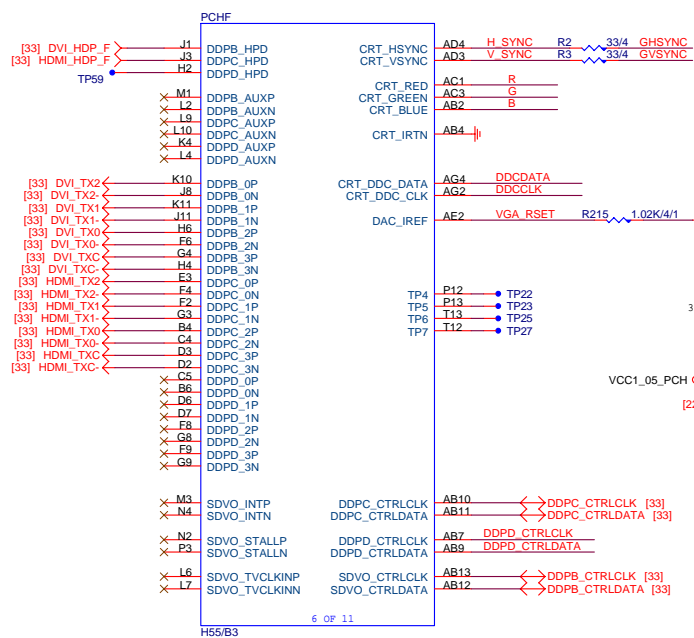
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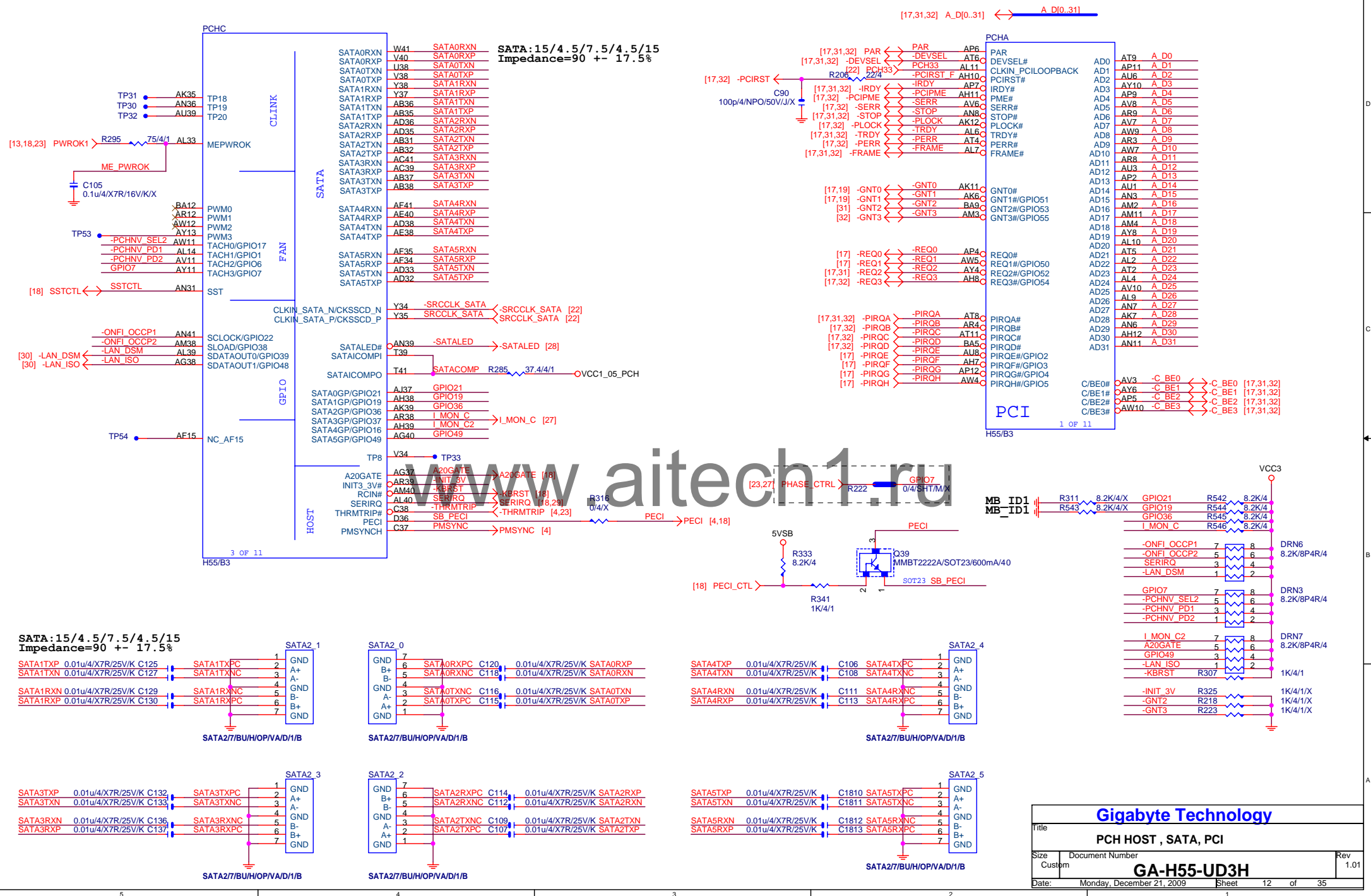
NV_PCH

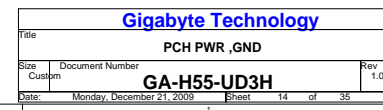
DMI Terminator voltage
HI : AC COUP : TX/RX TO VCC
LO : DC COUP : HALF SWING

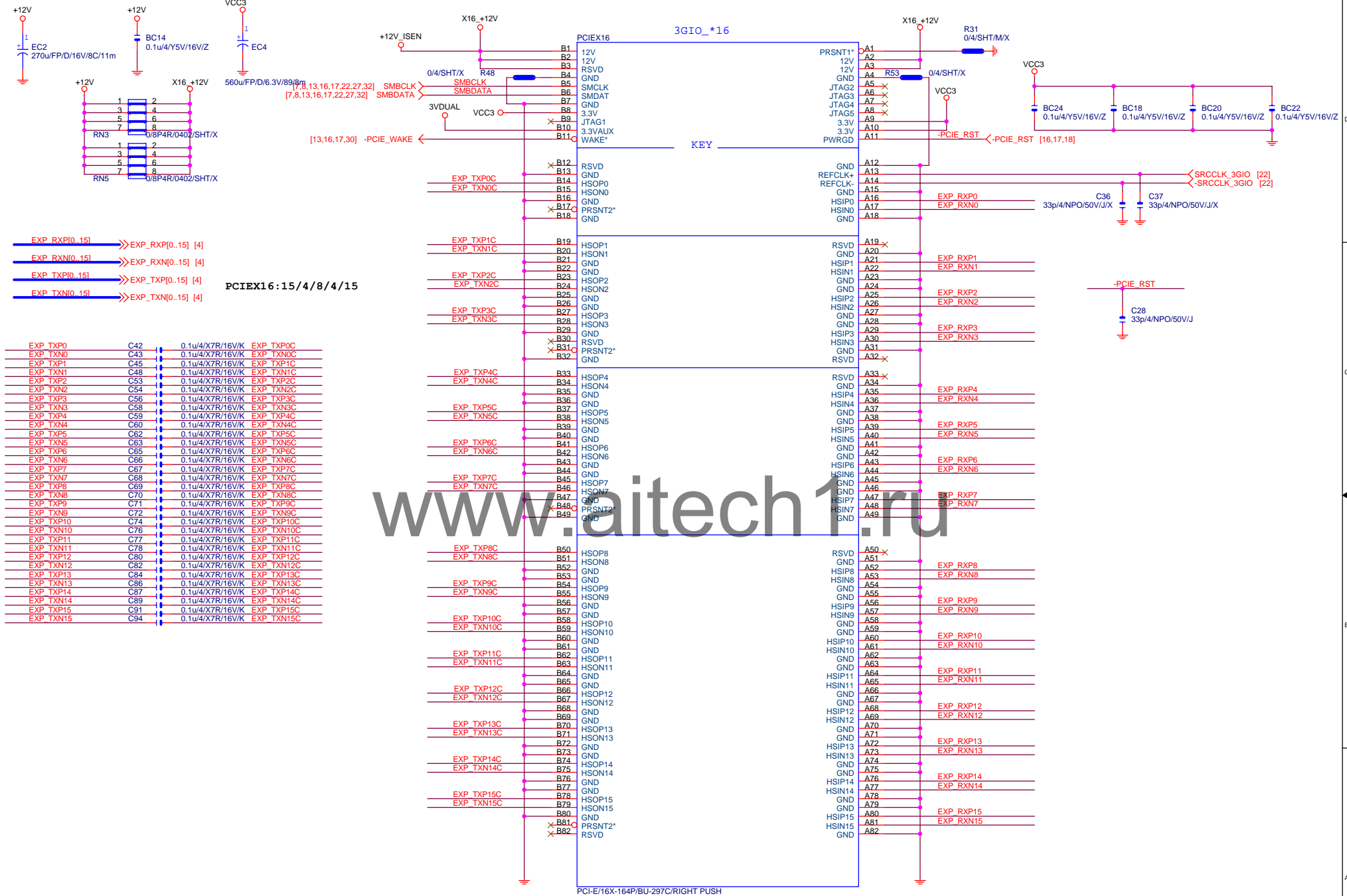
Gigabyte Technology

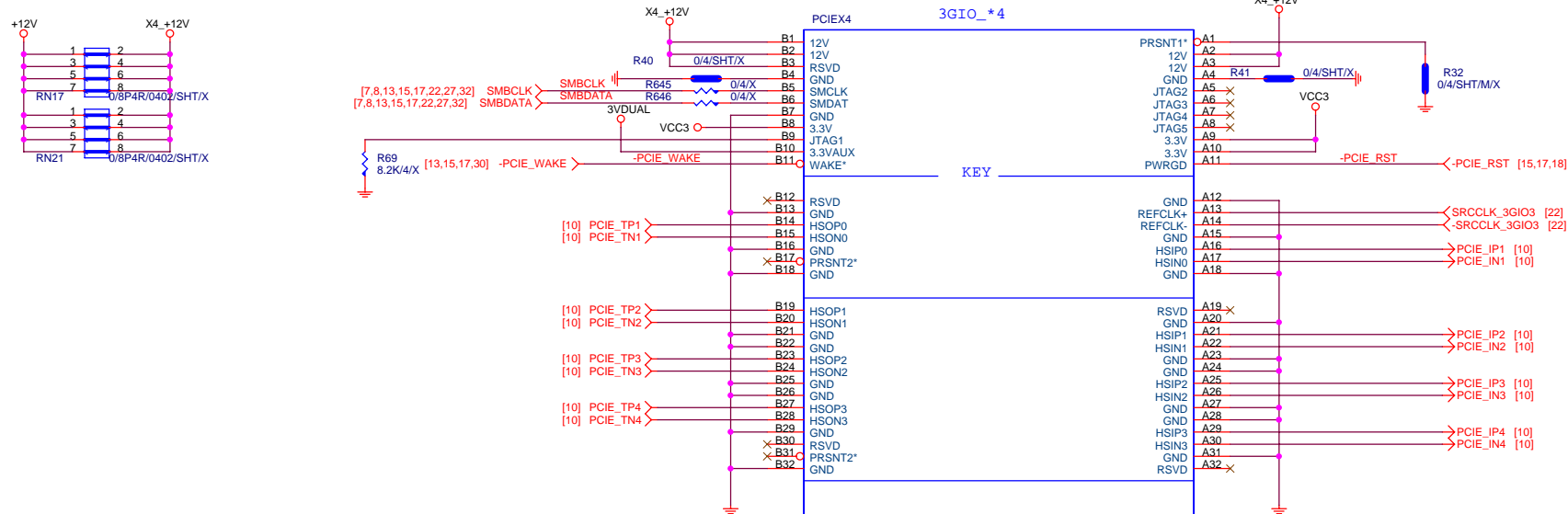
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Size	Document Number	Rev
B	GA-H55-UD3H	1.01
Date:	Monday, December 21, 2009	Sheet 10 of 35



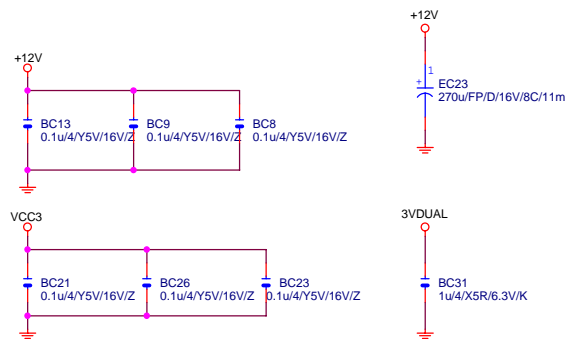








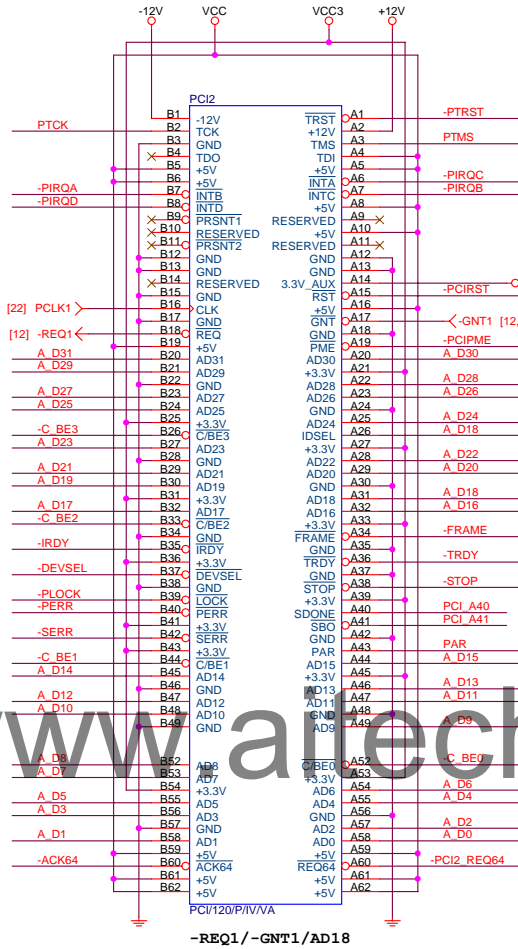
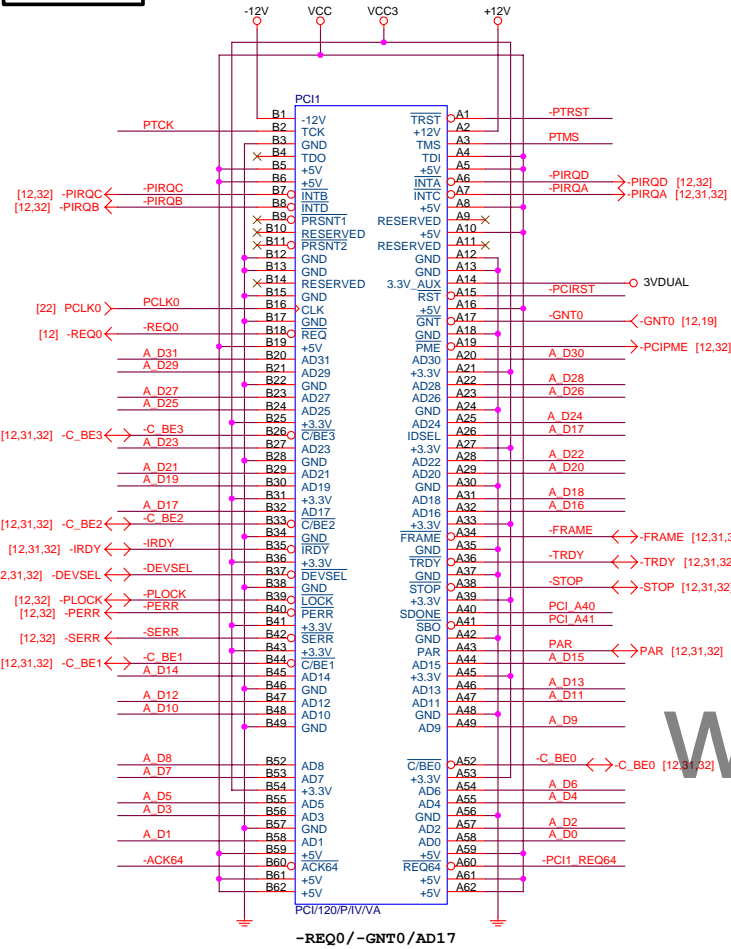
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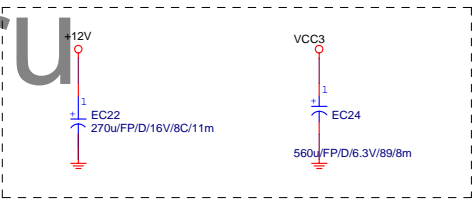
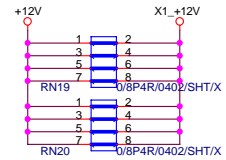
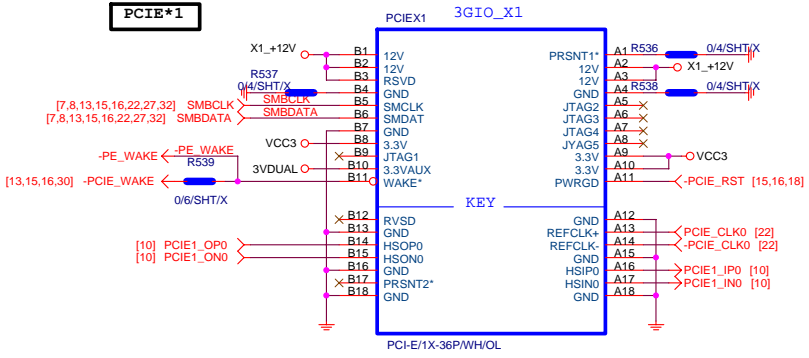
PCI-E/16X-65P/BU/RIGHT PUSH

Gigabyte Technology			
Title PCI EXPRESS X 4 PORT			
Size Custom	Document Number GA-H55-UD3H		Rev 1.01
Date: Monday, December 21, 2009	Sheet	16	of 35

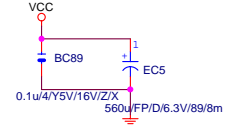
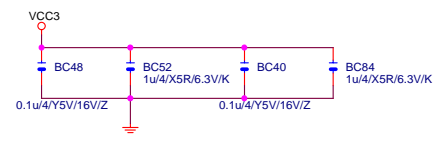
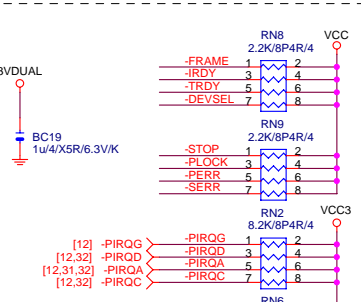
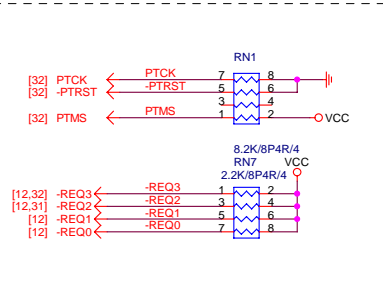
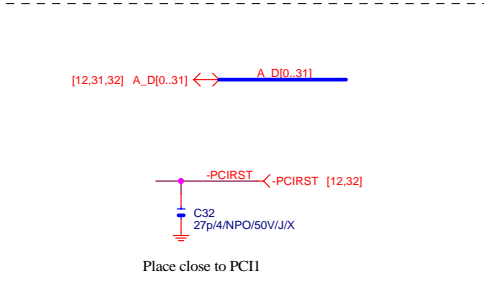
PCI1,2 SLOT

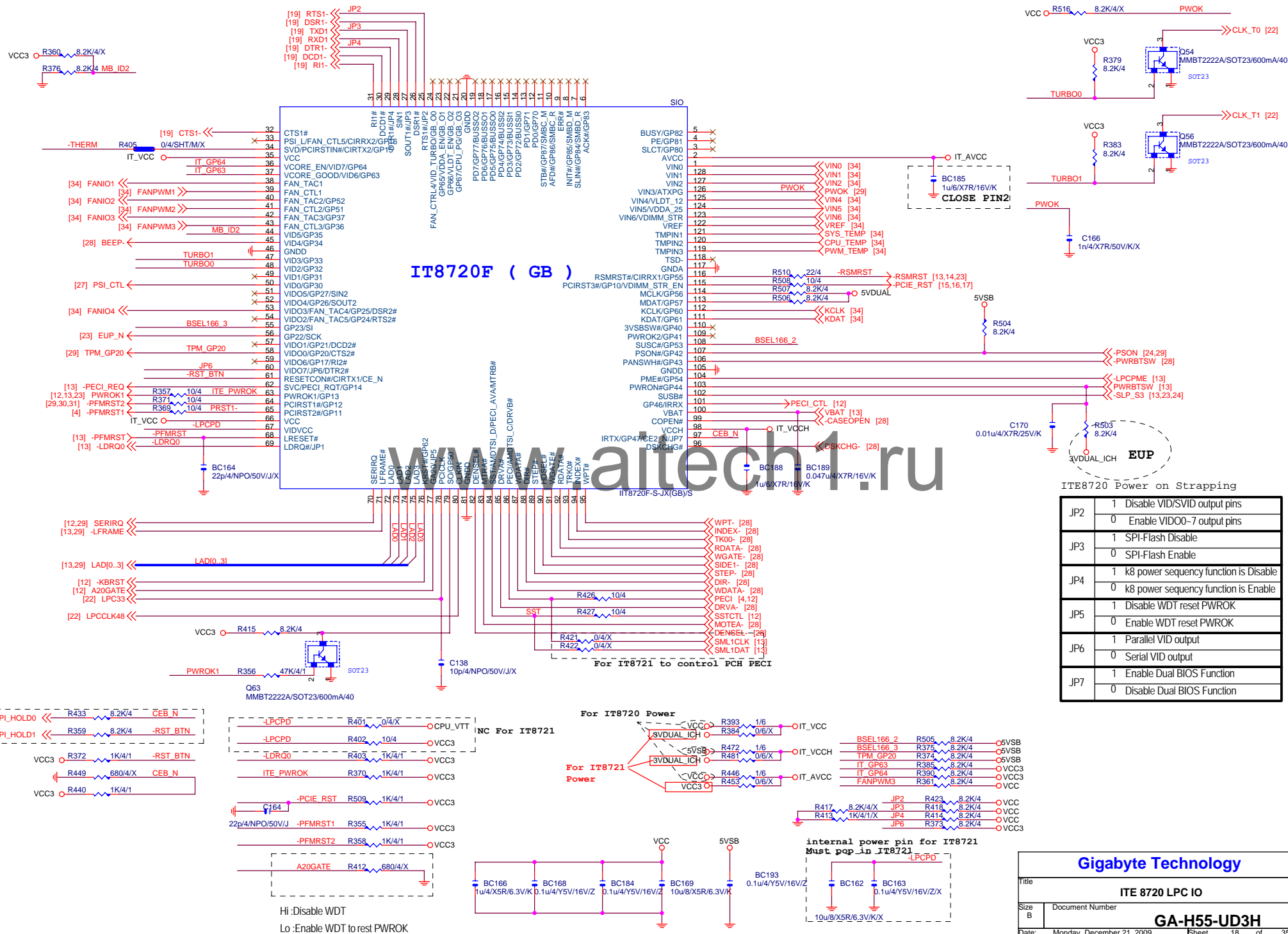


PCIE*1



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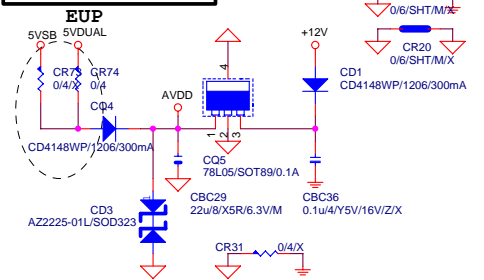


20K/4/0.1% @ALC889A
20K/4/1% @ALC889A+/ALC888Vx

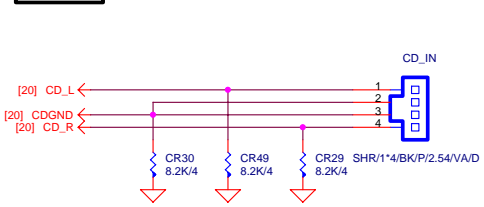


Can Support Amp Out

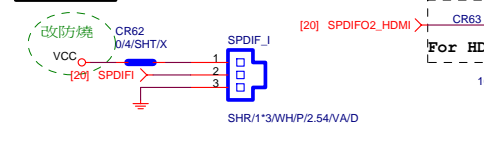
CODEC POWER/EMI PAD



CD IN

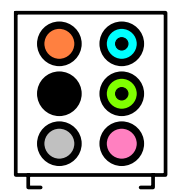


SPDIF_IN

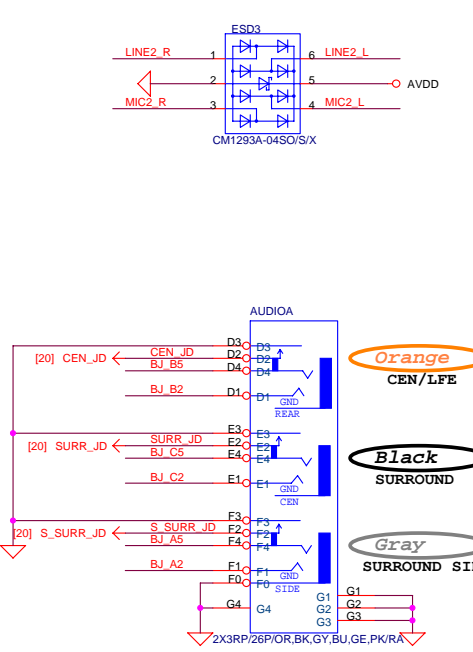
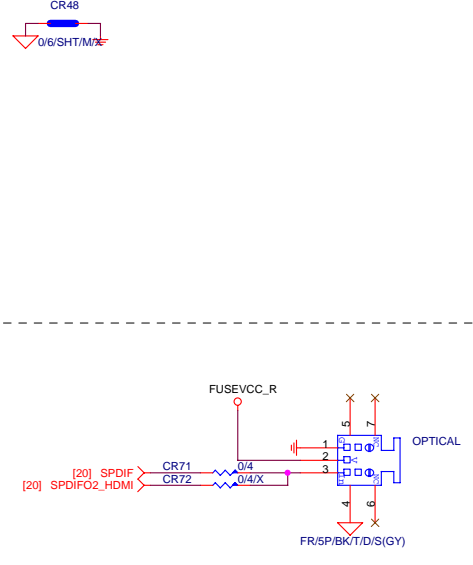
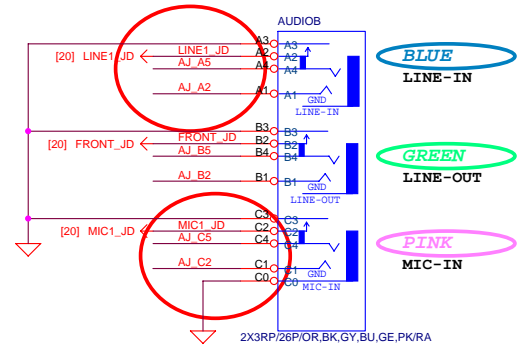


AZALIA JACK

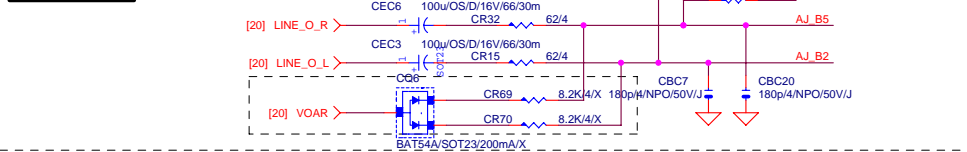
BTX AZALIA CONNECTOR



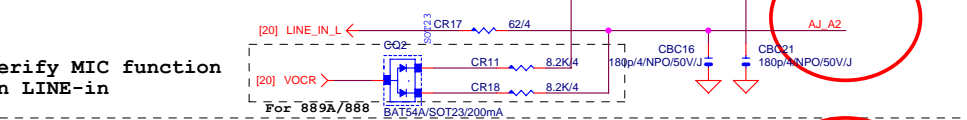
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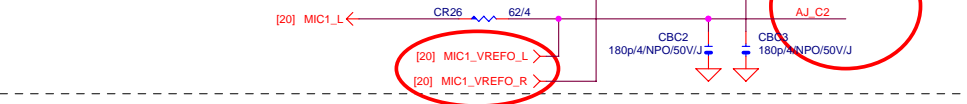
LINE-OUT



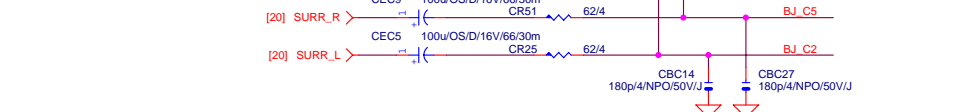
LINE-IN



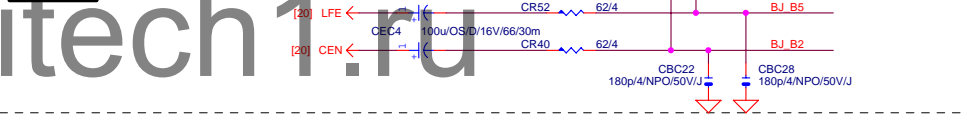
MIC-IN



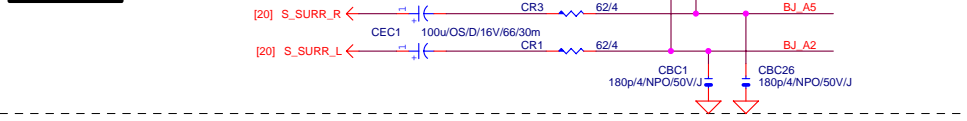
SURROUND



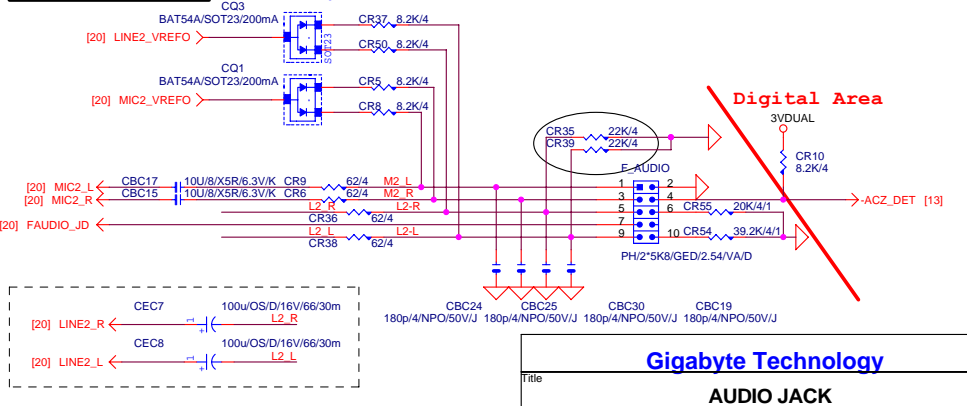
CEN/LFE



SURR BACK

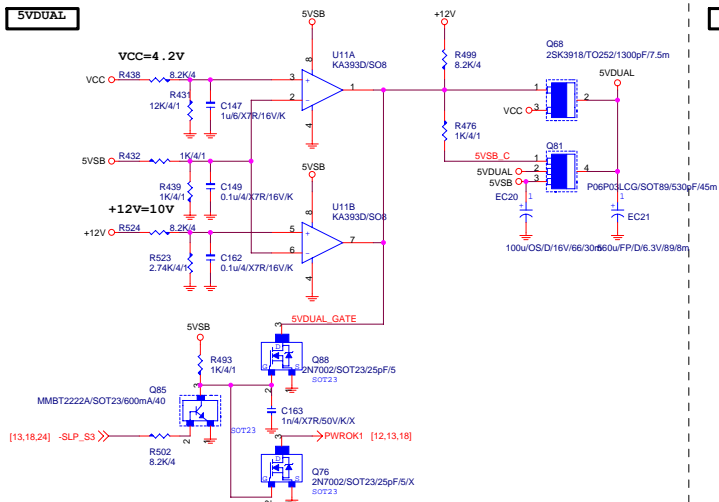


AZALIA FRONT PANEL

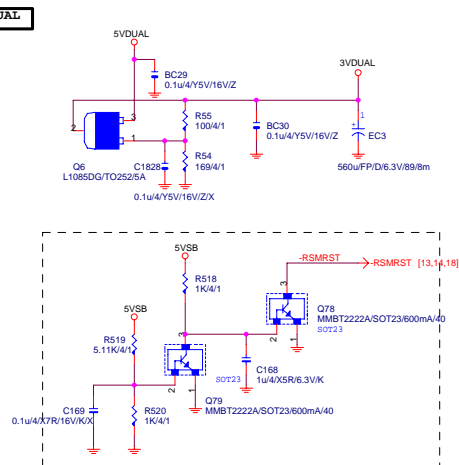


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Title			
AUDIO JACK			
GA-H55-UD3H			
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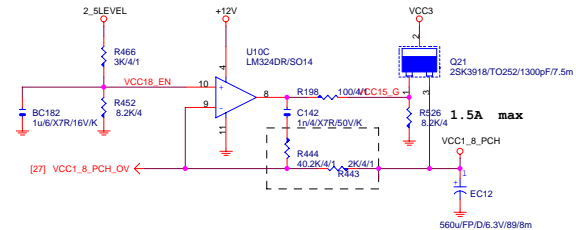
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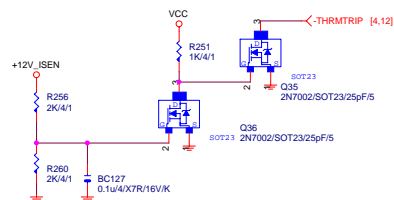
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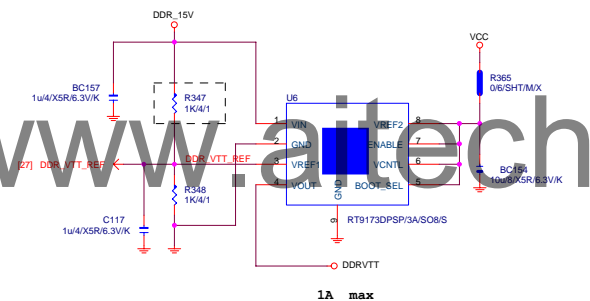
VCC1_8_PCH



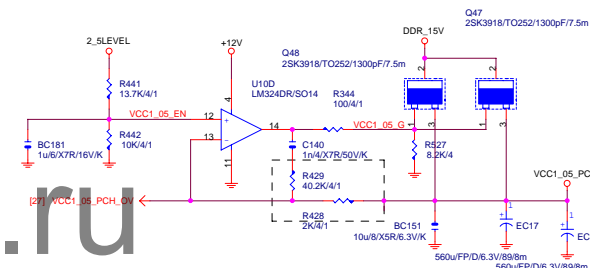
+12V SHORT PROTECT



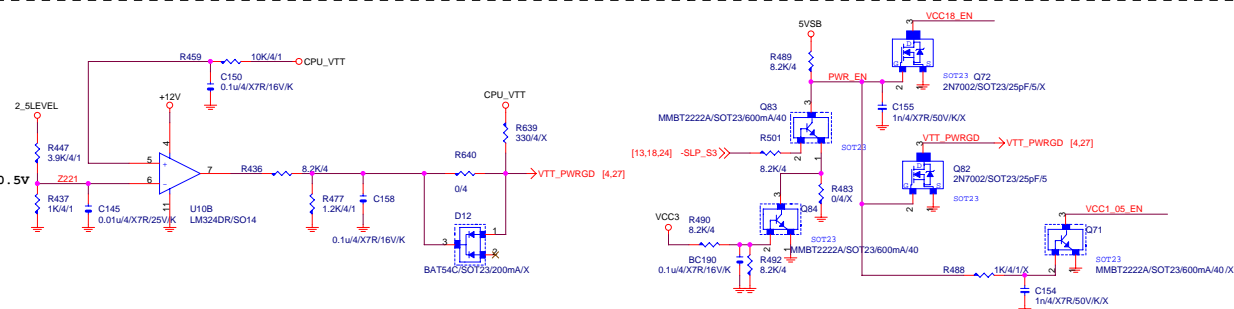
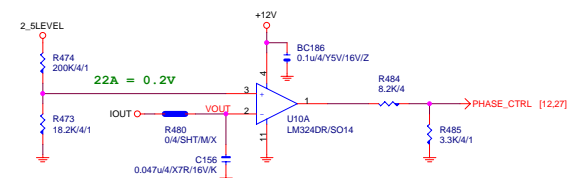
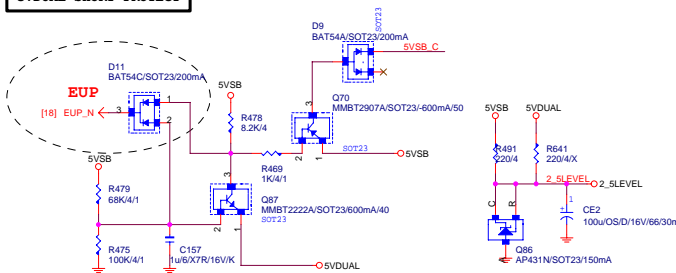
DDRVTT

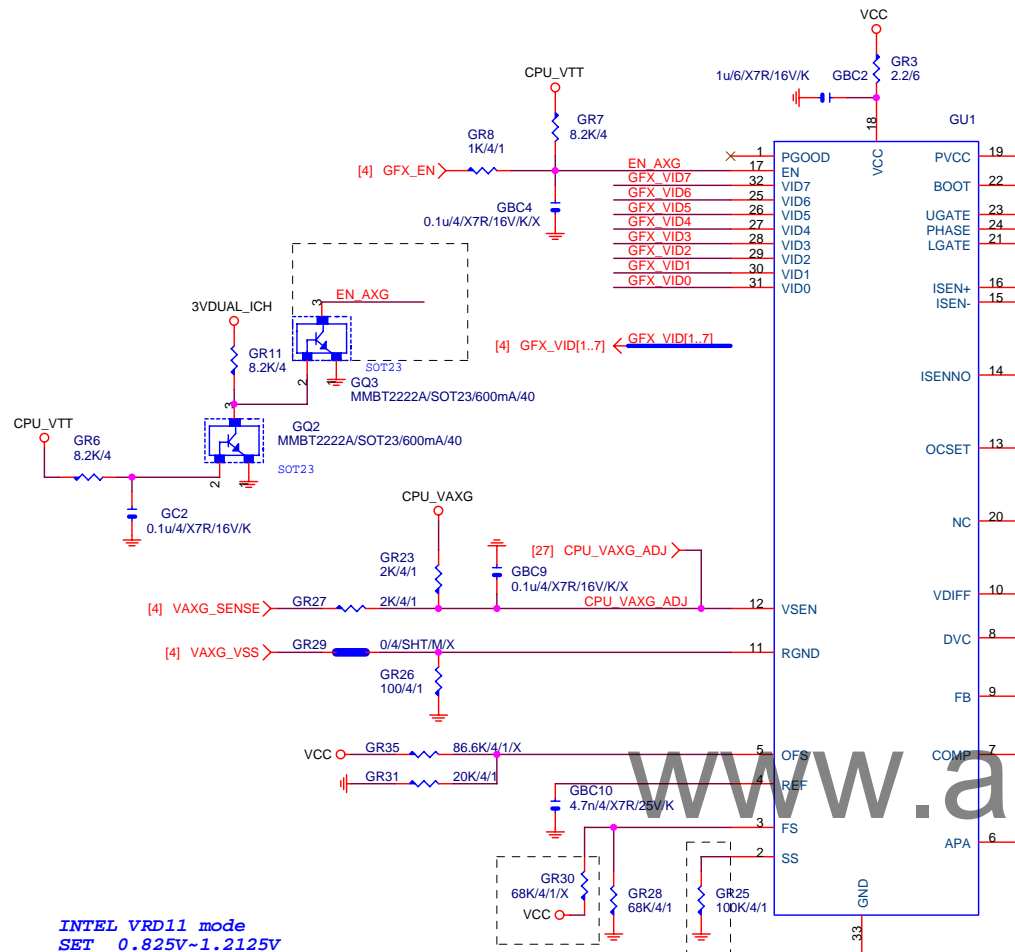


VCC1_05_PCH



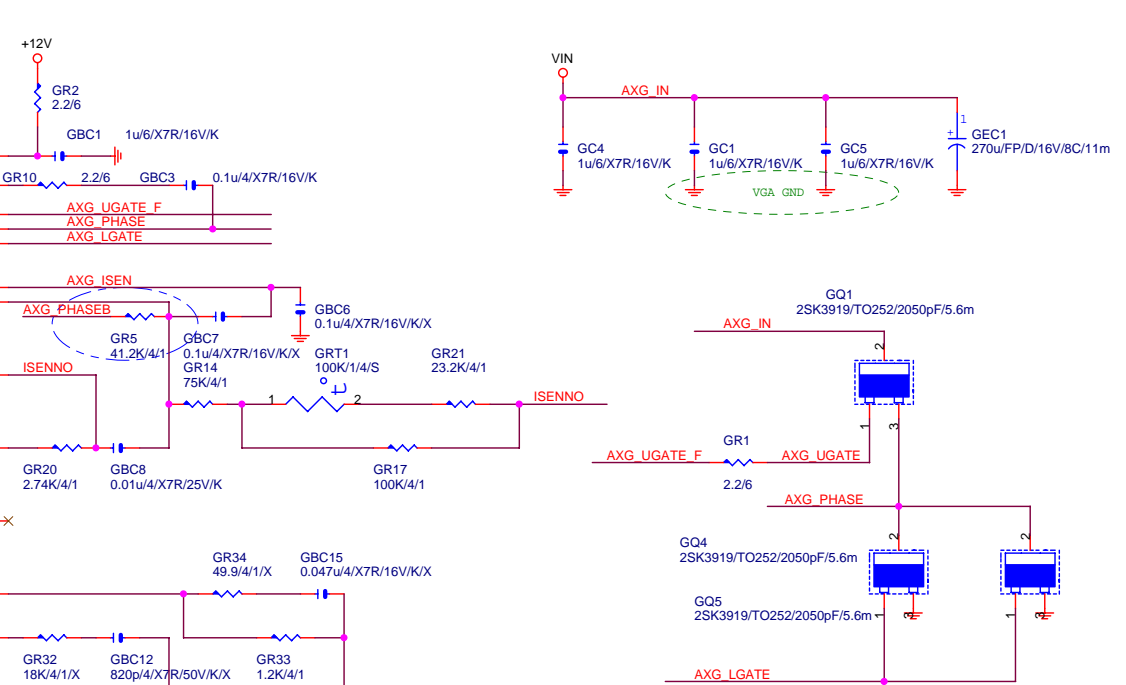
5VDUAL SHORT PROTECT



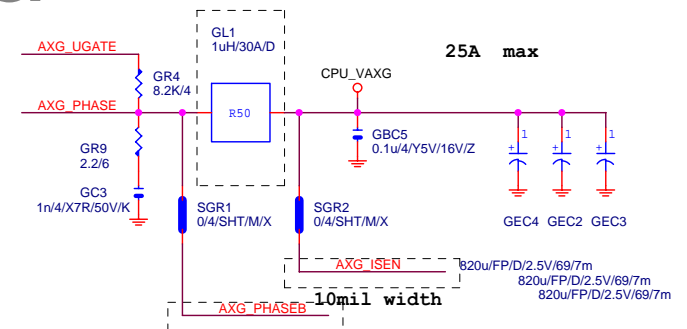


SS pin PD to set INTEL ISL6314CRZ-T/QFN32[10TA1-606314-01R]
VR11 mode

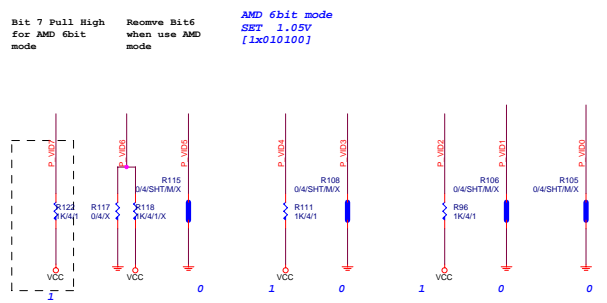
OCP點做在49A
 $R_{ocset}=R_{136}=2.74k$, $I_{sens}=94\mu A$, $R_s=R_{127}=8.25k$,
 $R_{comp}=R_{128}+[R_{135}/(DRT1+R_{129})]=78k$, $DCR=0.78mohm$
 $I_{ocp}=(R_{ocset}*I_{sens}*R_s/(R_{comp}*DCR))$
 $= (2.74k*94\mu A*8.25k)/(45K*0.97m)=49A$
 $R_t=10^{*}\{10.61-[1.035X\log(FS)]\}$ $R_t=R_{151}=68kohm$, $FS=380KHz$
 $OVP=VDAC+175mV$



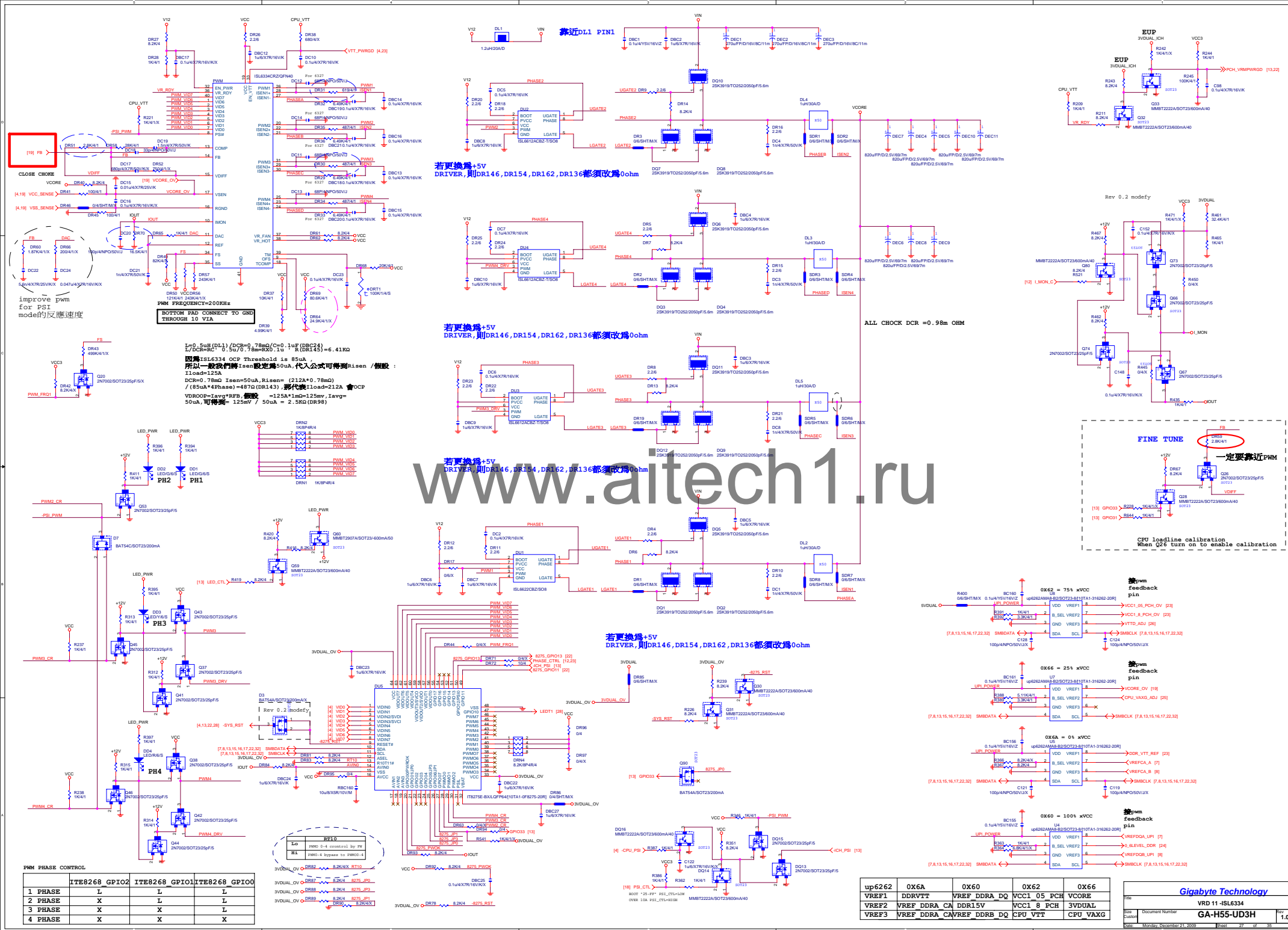
IAXG for 2009A FMB (73W TDP SKU support): 20A
IAXG for 2009B FMB (87W TDP SKU support): 25A

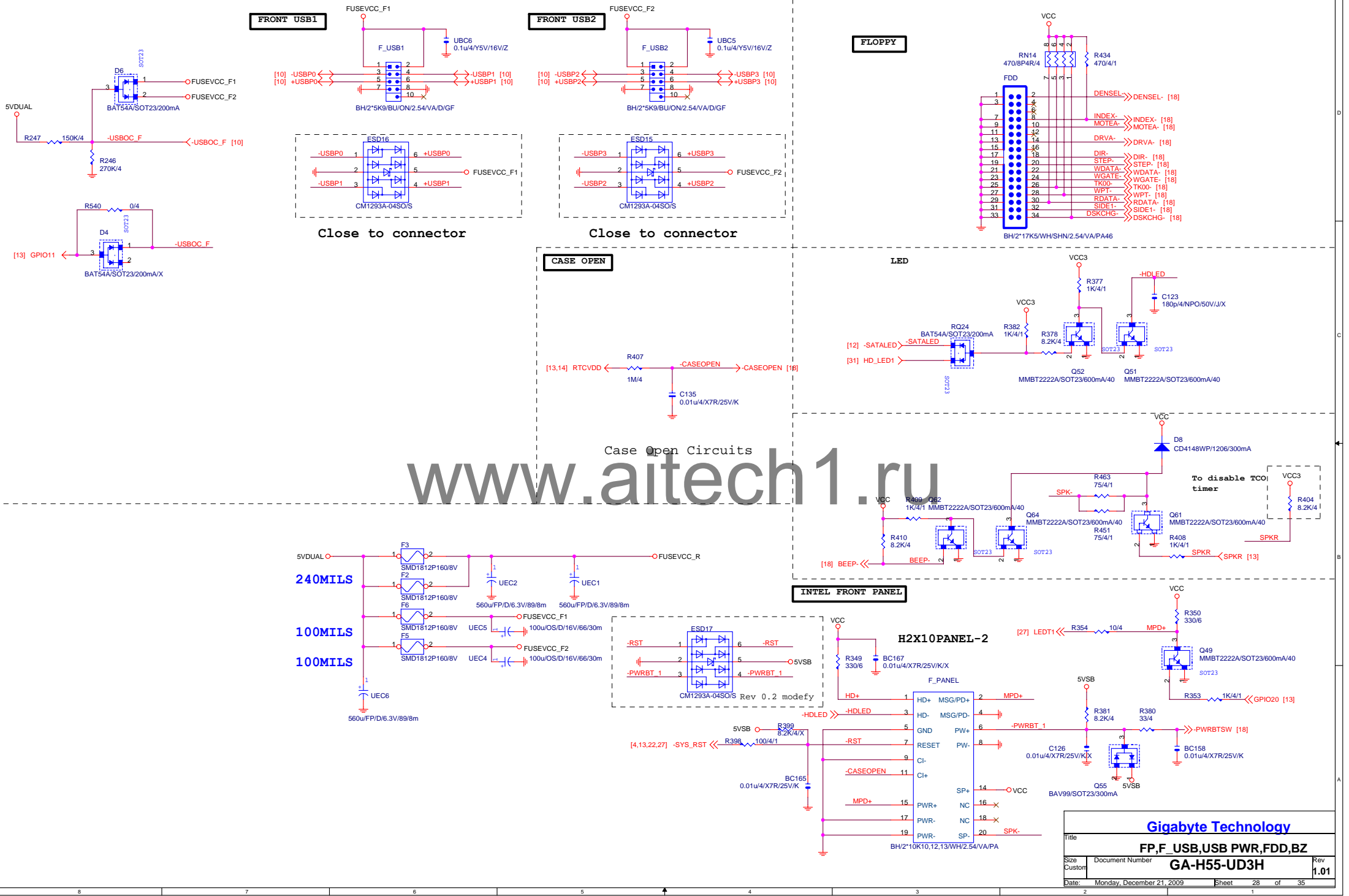


Gigabyte Technology			
Title			
CPU_VAXG_ISL6314CRZ			
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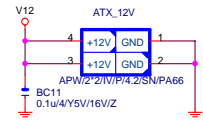


560uF/DP/D/6.3V/68/8m RIPPLE CURRENT=5.6A
Coefficient=1.7(85℃), 1(105℃)
VIN Ripple current=5.6X1.7=9.52A(85℃)
-->故固態電容須2X9.52=19.04>11.91A
1000uF/D/6.3V/8C/30m RIPPLE CURRENT=1.14A
Coefficient=1.7(85℃), 1(105℃)
VIN Ripple current=1.14X1.7=1.938A(85℃)
-->故電解電容須7X1.938=13.566>11.91A



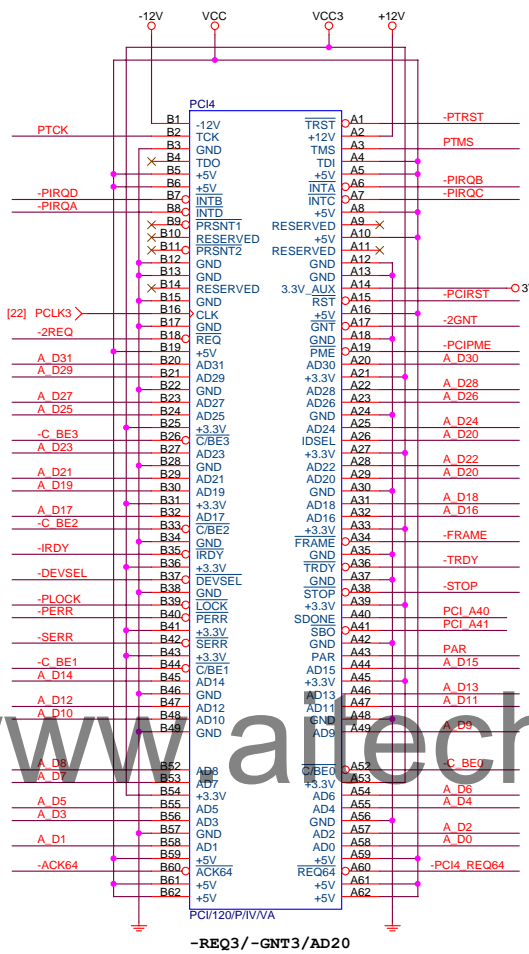
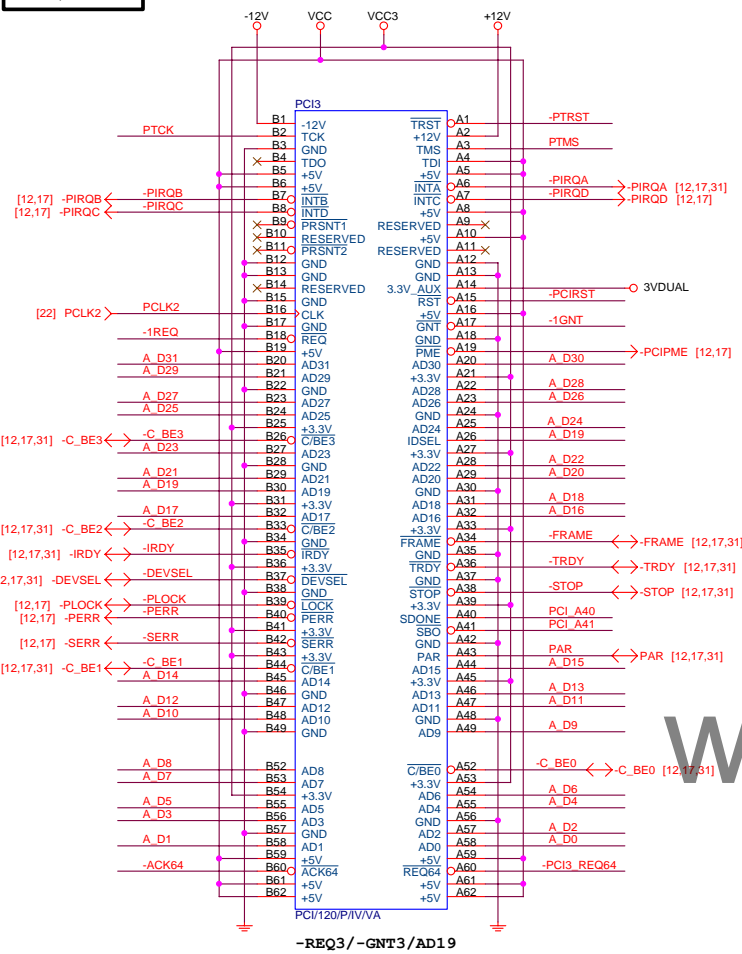


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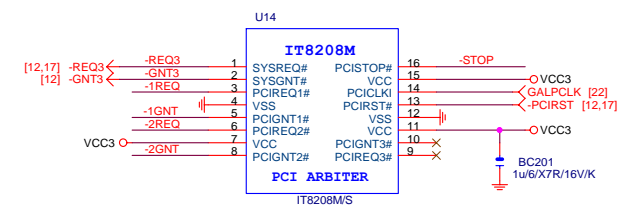
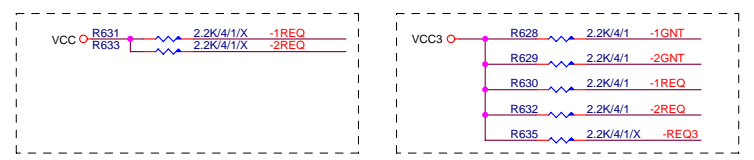
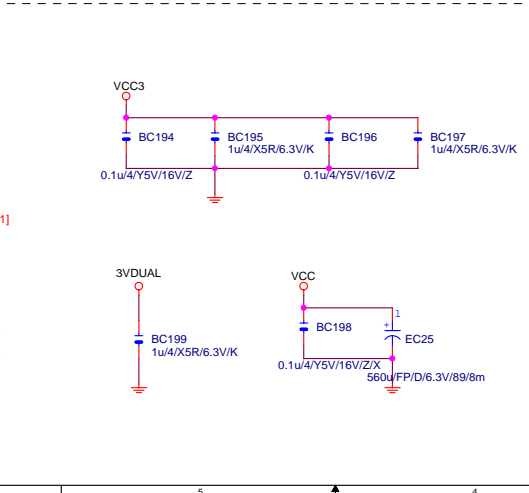
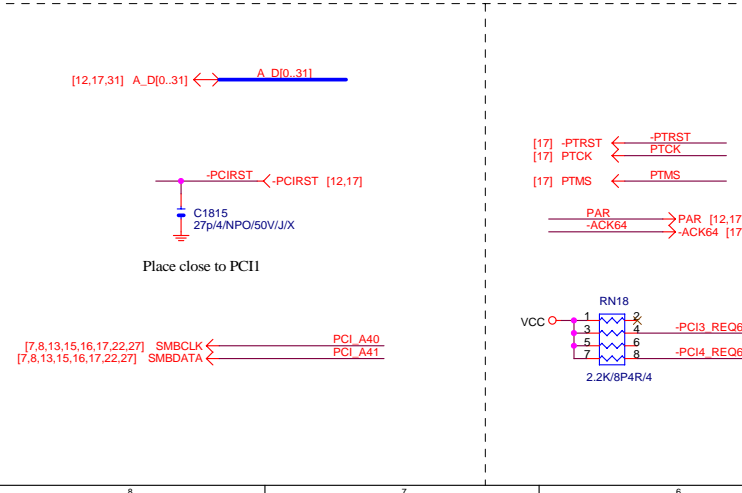
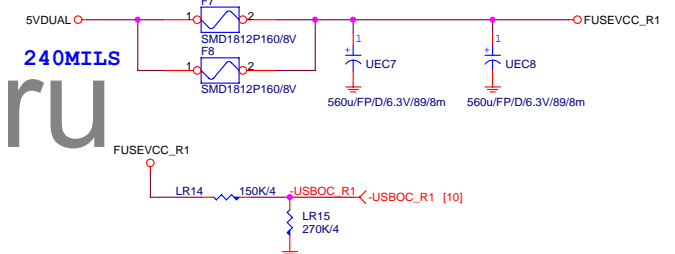
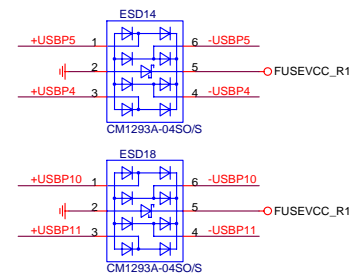
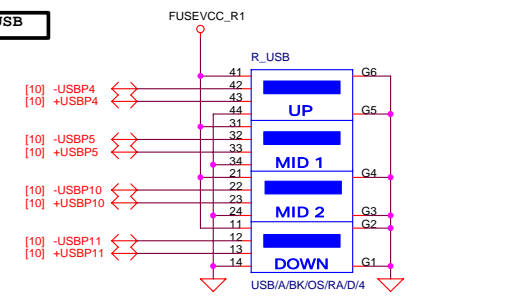


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ATX POWER CONNECTOR			
Size Custom	Document Number	GA-H55-UD3H	Rev 1.01
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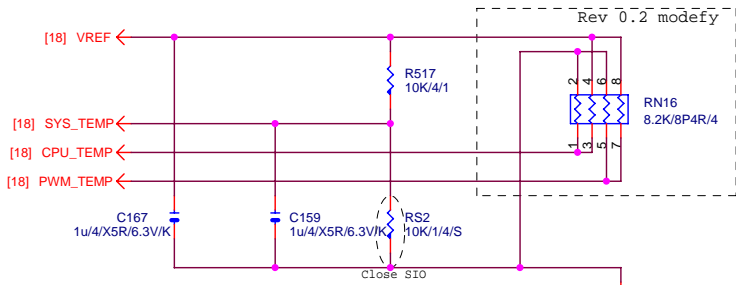
PCI1,2 SLOT



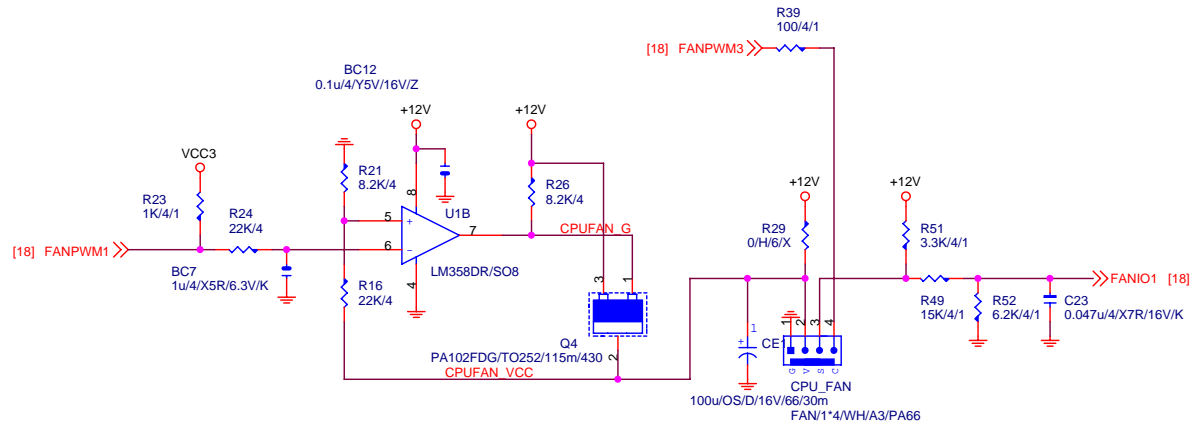
R_USB



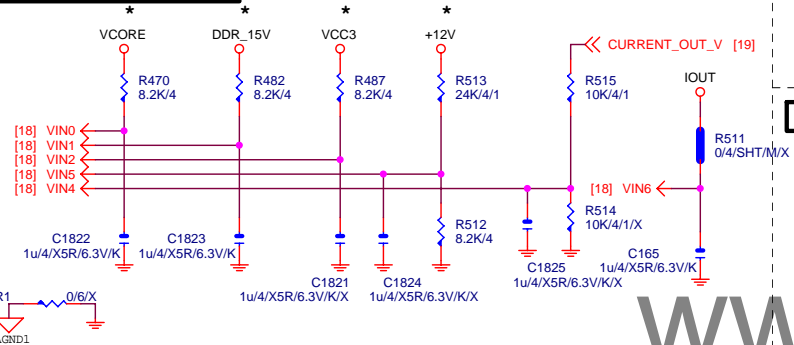
TEMP H/W MONITOR



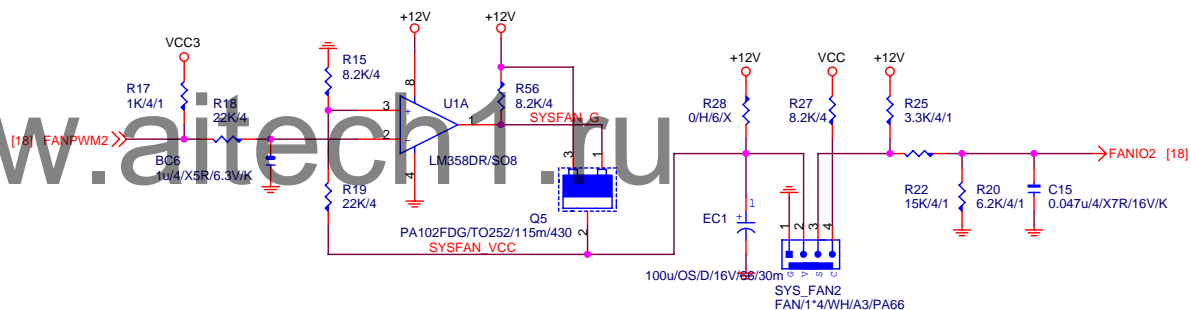
CPU SMART FAN



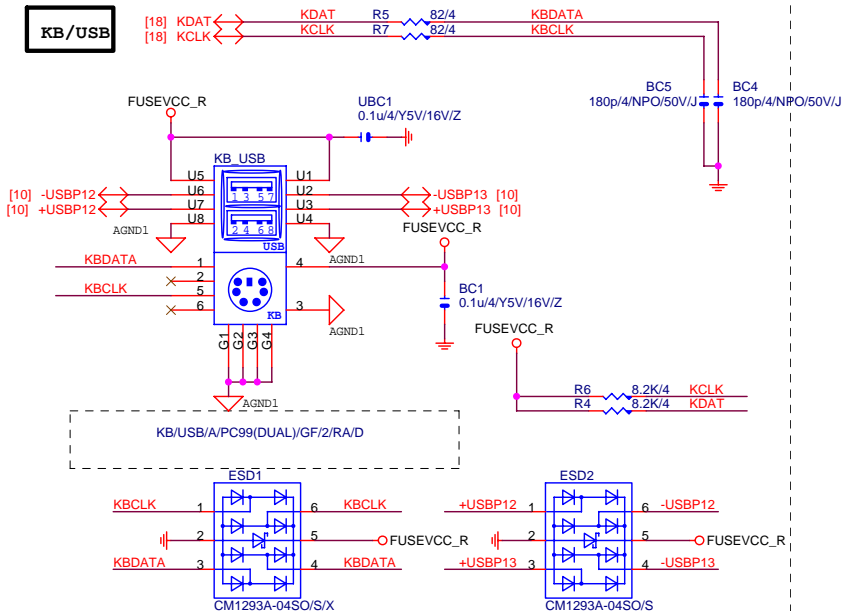
VOLTAGE-- H/W MONITOR



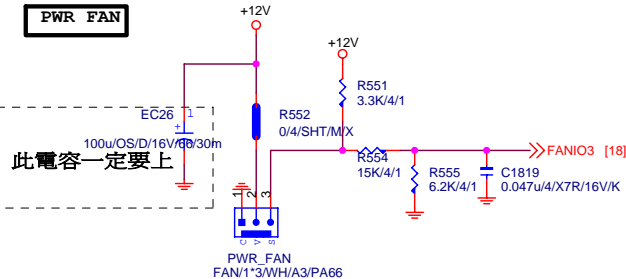
SYS SMART FAN Linear SYS_FAN



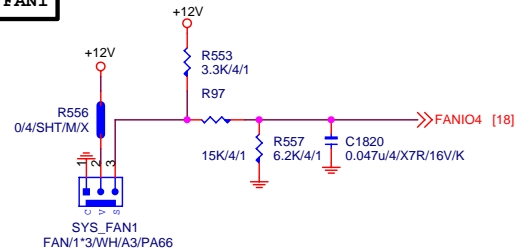
KB/USB



PWR FAN



SYS FAN1



Gigabyte Technology

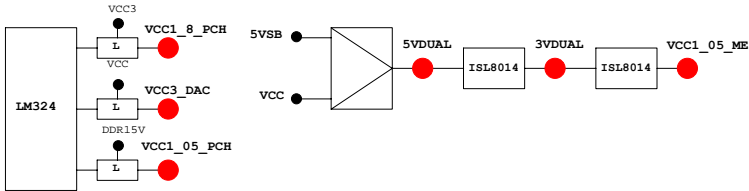
Title		HWM,KB/MS, FAN CTRL	
Size	Document Number	GA-H55-UD3H	
Custom		Rev 1.01	
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PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A	
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A	
GP2/PIRQE#	MAIN		GPI -PIRQE	P/U 8.2K VCC3	
GP3/PIRQF#	MAIN		GPI -PIRQF	P/U 8.2K VCC3	
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3	
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3	
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A	
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A	
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL	
GP9/OC5#	STBY		NATIVE OC5#	N/A	
GP10/OC6#	STBY		NATIVE OC6#	N/A	
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL	
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL	
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL	
GP14/OC7#	STBY		NATIVE OC7#	N/A	
GP15	STBY	L	GPO GPIO15	N/A	
GP16	MAIN		GPI -SKTOCC	P/U 8.2K VCC3	
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A	
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND	
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3	
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3	
GP21	MAIN		GPI VCC18_PCH_OV2	P/U 8.2K VCC3	
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3	
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3	
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL	
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL	
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL	
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL	
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL	
GP29	STBY	L	GPI GPIO29	N/A	
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL	
GP31	STBY	H-Z	GPI N/A (Reverse)	P/U 8.2K VCC3	
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND	
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3	
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3	
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3	
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3	
GP37	MAIN		GPI N/A	P/U 8.2K VCC3	
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3	
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3	
GP40	STBY		NATIVE OC1#	N/A	
GP41	STBY		NATIVE OC2#	N/A	
GP42	STBY		NATIVE OC3#	N/A	
GP43	STBY		NATIVE OC4#	N/A	
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL	
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL	
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL	
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL	
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3	
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3	
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC	
GP51	MAIN	H	NATIVE -GNT1	N/A	
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC	
GP53	MAIN	H	NATIVE -GNT2	N/A	
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC	
GP55	MAIN	H	NATIVE -GNT3	N/A	
GP56	STBY		NATIVE N/A (Reverse)	P/U 8.2K 3VDUAL	
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL	
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL	
GP59	STBY		NATIVE USB_OC0#	N/A	
GP60	STBY	H-Z	NATIVE N/A (Reverse)	P/U 8.2K 3VDUAL	
GP61	STBY	L	NATIVE -SUSTAT	N/A	
GP62	STBY	L	NATIVE SUSCLK	N/A	
GP63	STBY	L	NATIVE GPIO63	N/A	
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A	
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A	
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A	
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A	
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL	
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL	
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL	
GP75	STBY	H-Z	NATIVE N/A (Reverse)	P/U 8.2K 3VDUAL	

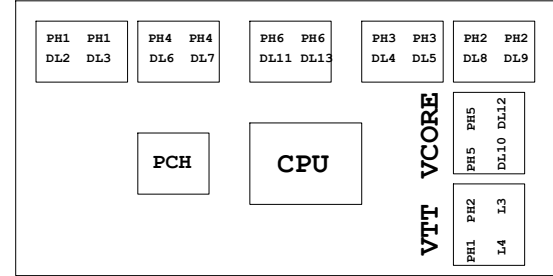
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PWRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AED#/GP86/SMBD_R	2X_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBD_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VID04/GP26/SCUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組) 包材階

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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